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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,926	03/30/2001	Giovanni Campardo	856063.689	7548

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EXAMINER
YUFA, ALEKSANDR L

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,926	CAMPARDO ET AL.	
	Examiner	Art Unit	
	Alex L. Yufa, Ph.D.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to under 37 CFR 1.71, as being so incomprehensible as to preclude a reasonable search of the prior art by the examiner. For example, the following items are not understood: the step of "loading test data and/or instructions into..." claimed in the claim 1.

Drawings

The drawing is objected to as failing to comply with 37 CFR 1.84(p)(3).

New corrected drawings are required in this application because:

a) the numbers should not be underlined (see 3 and 7);

b) the drawing has to be marked as Figure.

The corrected drawings are required in reply to the Office action.

Claim objection

2. Claims 14-15 are objected under 37 CFR 1.126. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution.

Two last claims are not numbered in sequence.

Appropriate correction is required.

Claim Rejection

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-5 are rejected under 35U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in specification in such way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1: a single step claim, i.e. "loading test data and/or instructions into ...", where a step recitation does not appear in combination with another recited step of method, is subject to an undue breadth rejection under 35U.S.C. 112, first paragraph. Claims 2-5 depend from respective claim 1, hence inherit the deficiencies in claim 1.

Claim

Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-5 provide for the use of method, but, since the claims do not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. The claims are indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced, i.e. limitation in claims 2-5 are recite the means, but not the steps of the claimed method.

The Examiner interprets claims 1-5 as being similar to claims 6-15.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6-8 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in view of Bond et al. (US 4,450,559).

Referring to claim 6, Mullarkey teaches to use "an integrated memory device 10" (see Fig.1) comprising "a memory array 12", including "a plurality of memory cells 22", "control circuit 16", and "a test mode 20" provided for operating the memory device 10 in a test regime.

Mullarkey does not explicitly point out to use two memories, but Bond et al. teaches to comprise two memories: "main memory system 11" and "secondary memory unit 13" (see Fig.1) coupled with the "electronic control system (ECC) 10". Bond et al. does not explicitly point out that both of memories are internal, inherently teaching for any combinations (internal/external) of two memories. Also, it is well known that mostly integrated circuits do not contain the test operation memory (accept some specific integrated circuit particularly intended, e.g. for memory testing).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mullarkey with the teaching of Bond by simply using one memory as internal and second memory as external, because one of ordinary skill in the art would simply use an external memory for the test of the memory into integrated circuit to provide minimization of the integrated circuit (IC) dimensions, universality of application, and convenience for the test equipment.

Claims 7, 8 depend from respective claim 6, hence inherit the rejection in claim 6. Also, according to claim 7, Mullarkey teaches to use the "input/output circuits 18" (column 3, lines 41, 42) and contacts (e.g. "contact 99" /see column 8, line 32, and

Fig.6/) for connections. Additionally, it is well known that the integrated circuits and/or electrical/electronic devices are provided with data pins and/or address pins for connection of the integrated circuit (IC) and/or electrical/electronic devices, and explicitly pointed out and disclosed, for instance, in device by Mullarkey. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply to use Mullarkey's input/output circuit and/or contacts for connection, because one of ordinary skill in the art with the teaching of Mullarkey by including use the contacts (pins) for electrical connection of the external electronic components, because (IC) are obviously needed to be electrically connected to the PCB (Printed Circuit Board) and/or test equipment, that can be provided the use of pins and/or contacts.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in view of Kumakura et al. (US 5,566,386). Applicant claims the nonvolatile type of the external memory unit 7. Mullarkey does not explicitly teach and point out to nonvolatile memory, inherently teaching to use any kind of memory, but Kumakura et al. teaches to use "a nonvolatile semiconductor memory and a test method for the same" (e.g. , see a title and cross specification)

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mullarkey with the teaching of Kumakura by using inherently any kind of memory for testing, including the nonvolatile memory, because the memory test equipment, providing the test of the memory and control logic operability, mostly (by their purpose and application) is

developed as an universal device for testing of the different kinds of integrated memory circuits, logically including the nonvolatile memory.

Claims 9-13 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in view of Kumakura et al. (US 5,566,386).

Referring to claim 9, the device by Mullarkey et al. Includes the "memory array 12", "control means 16" and "test mode 20" (column 3, lines 40-43), Mullarkey does not explicitly teach and point out to the external test control, but teaches to use a control circuit 16, a test mode 20 and appropriate memory array (inherently internal) 12, including a plurality of "memory cells 22" (column 3, line 49), provided for operating the memory device 10 in a test regime.

Kumakura at el. teaches to comprise the test control means including "operation logic circuit 3", "command register 2" (column 6, lines 61, 62), "test cell 19", "switching circuit 7" (column 6, line 64), "timing generating circuit 10", "erasure source control circuit 18" (column 7, line 8), and other analogous means presented in the applicant's claims. Also, it is well known that some integrated circuits do not contain the test control device (accept specific integrated circuit particularly intended, e.g. for memory testing devices).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mullarkey with the teaching of Kumakura by using the test control device as a testing equipment, because mostly the test control devices are external apparatus, and it is well known and

obvious, that test control devices can include the circuit for simulating the internal memory array in order to provide maximally efficient test of the internal memory operability.

Claims 10, 11 depend from respective claim 9 hence inherit the rejection in claim

Also, claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. US 5,732,033). Mullarkey teaches to use the input/output circuits 18 (column 3, lines 40, 41) and contacts (e.g. contact 99 /see column 8, line 32 and Fig.6/) for connections. Additionally, it is well known that the integrated circuits and/or electrical/electronic devices can be provided with the contacts or connector for detachable connection, for instance, by a socket. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply to use Mullarkey's input/output circuit and/or contacts/connectors for connection, because one of ordinary skill in the art with the teaching of Mullarkey by including use the detachable connection (e.g. connector) for electrical connection of the external electronic components (e.g. semiconductor substrate) to, for example, PCB and/or test control unit in order to provide sufficient universality of the test equipment .

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. US 5,732,033) in view of Kumakura et al. (US 5,566,386). Mullarkey et al. teaches, that the memory device comprises the circuit for simulating the memory array and the circuit for simulating the control logic circuit integrated into test device ("invention provides an arrangement for rapidly equilibrating the paired digit lines of the memory

array of a semiconductor memory device, such as a dynamic random access memory device", e.g., see column 9, lines 20-24), during testing of the memory device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply to use Mullarkey's integrated means, because one of ordinary skill in the art with the teaching of Mullarkey by including circuit for simulating the internal memory array and the circuit for simulating the control logic circuit into test device, that is mostly the regular procedure for internal memory array test providing the efficient memory test result.

Referring claims 12, 13, Mullarkey et al. teaches, that the memory device comprises the circuit for simulating the memory array. Mullarkey et al. does not limit and/or explicitly point out the memory array location, inherently teaching to use any and all possible locations of the memory array.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply to use Mullarkey's memory array, for example, as an external, because one of ordinary skill in the art with the teaching of Mullarkey by including circuit for simulating the internal memory array into test device, that is mostly the regular procedure for internal memory array test providing the efficient memory test result by external memory array, located into the test equipment.

Claims 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumakura et al. (US 5,566,386).

According to claim 14, Kumakura et al. teaches to operate (simulate) the test control means including "operation logic circuit 3", "command register 2" " (column

6, lines 61, 62), "test cell 19", "switching circuit 7" (column 6, line 64), "timing generating circuit 9", "erasure source control circuit 18" " (column 7, line 8), and other analogous means presented in the applicant's claims. Kumakura does not explicitly teach and point out to the external location of any or some means, inherently teaching to use a control circuit 16, a test mode 20 and appropriate memory array (inherently internal) 12, including a plurality of memory cells 22, for operating the memory device 10 in a test regime.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kumakura with the teaching of by using the external location of any/some means for memory test, because it is obvious and well known, that the procedure for most tests and particularly for memory test control apparatus includes steps of simulating the circuits, performing the test, and observing interactions and results, considering the purpose of the testing equipment.

Referring to claim 15, Kumakura et al. teaches to operate (simulate) the test control means including "operation logic circuit 3", "command register 2", "test cell 19", "switching circuit 7", "timing generating circuit 9", "erasure source control circuit 18", and other analogous means presented in the applicant's claims. Kumakura does not explicitly teach and point out to the external location of any or some means, inherently teaching to use a "control circuit 16", "a test mode 20" and appropriate "memory array (inherently internal) 12", including a plurality of "memory cells 22", for the memory device 10 in a test regime.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kumakura with the teaching of by using the external location of any/some means for memory test, because it is well known and follows from the IC technology ideology, that in order to increase degree of IC's integration and universality they do not include the test circuits (except some specific IC), and obviously such means for memory test have to be externally located into test apparatus

Claims 1-5 are similar to claims 6-15, and are rejected based on the same rationale thereof.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure 5,768,206.

The following are suggested formats for either a Certificate of Mailing or Certificate of Transmission under 37 CFR 1.8(a). The certification may be included with all correspondence concerning this application or proceeding to establish a date of mailing or transmission under 37 CFR 1.8(a). Proper use of this procedure will result in such communication being considered as timely if the established date is within the required period for reply. The Certificate should be signed by the individual actually depositing or transmitting the correspondence or by an individual who, upon information and belief, expects the correspondence to be mailed or transmitted in the normal course of business by another no later than the date indicated.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex Yufa whose telephone number is (703) 305-0715. The examiner can normally be reached on M-F at 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 746-7240.

aly
September 4, 2003

Alex L. Yufa, Ph.D.

Examiner

Art Unit 2133

Guy J. Lamarre
for
Albert DeCady
Primary Examiner